# Waveform analysis of the bridge type SFCL during load changing and fault time

AUTHOR(S):

Salim, KM; Hoshino, T; Kawasaki, A; Muta, I; Nakamura, T

CITATION:

Salim, KM ...[et al]. Waveform analysis of the bridge type SFCL during load changing and fault time. IEEE TRANSACTIONS ON APPLIED SUPERCONDUCTIVITY 2003, 13(2): 1992-1995

ISSUE DATE:

2003-06

URL:

http://hdl.handle.net/2433/39947

# Waveform Analysis of the Bridge Type SFCL During Load Changing and Fault Time

Khosru Mohammad Salim, Tsutomu Hoshino, Akio Kawasaki, Itsuya Muta, *Member, IEEE*, and Taketsune Nakamura

***Abstract*—DC reactor type SFCL has drawn the interest of some researchers in developing such device and more research work is being carried out in order to make it practically feasible. We have pointed out one issue that is not properly examined yet on such a device during load changing time. As we know, it is very difficult to introduce DC bias voltage to the reactor coil of the bridge type SFCL, some researchers are developing such device without using DC bias current. In such a case, the voltage drop occurs at the load terminal during the load increasing time caused by the DC reactor's inductance. By using the Electro-Magnetic Transients in DC systems which is the simulator of electric networks (EMTDC) software we carried out analysis of first few half cycles of the voltage and current waveforms after the load is increased. We also performed the same analysis for fault conditions. The peak value of the waveforms is considered in calculating the voltage drop at load terminal during the load changing time. The analysis can be used in selecting an appropriate inductance value for designing such SFCL.**

***Index Terms*—Bridge type, DC reactor, fault current limiter, superconductor.**

## I. Introduction

In A bridge type superconducting fault current limiter, it is very difficult to introduce a DC bias voltage inside the bridge. Some researchers are interested in designing such SFCL without using DC bias voltage [1]. If DC bias voltage is not used, selecting a proper inductance value is very important in this type of SFCL. From an economical point of view, lower inductance value means lower investment cost due to smaller length of superconductor coil. However, a lower inductance value would not reduce the fault current so much. On the other hand, higher inductance values cause a voltage sag during load increasing time [2]–[4]. So, optimum value is required. In this paper we analyze the load voltage waveforms at the time of load change by varying the inductance value. We also analyzed the fault current waveforms at the time of a fault and plotted the fault to normal current ratio at different inductance values. The DC shift occurrence in the current waveform is a common phenomena during fault time. A DC shift occurs depending on the fault instant of the current waveform. The maximum DC shift occurs when the fault is made at a zero crossing time. We have shown how the fault current is influenced by a DC shift when the fault is made at a zero crossing and at the peak position of the current waveform.

Manuscript received August 6, 2002.

The authors are with the Graduate School of Engineering, Kyoto University, Yoshida Honmachi, Sakyo, Kyoto 606-8501, Japan (e-mail: khosru@audrey.kuee.kyoto-u.ac.jp; kawasaki@audrey.kuee.kyoto-u.ac.jp; hoshino@asl.kuee.kyoto-u.ac.jp; muta@kuee.kyoto-u.ac.jp; tk_naka@kuee.kyoto-u.ac.jp).

Digital Object Identifier 10.1109/TASC.2003.812960

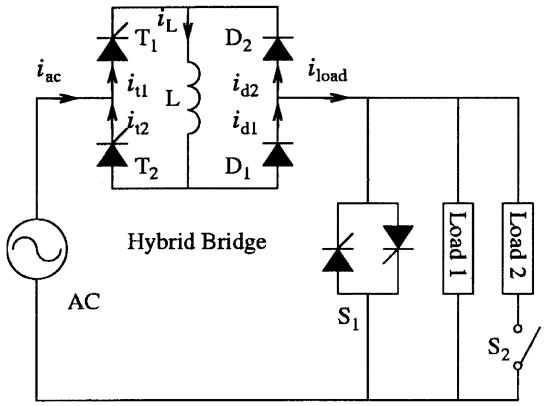


Fig. 1. Circuit diagram of bridge type SFCL used for analysis.

The circuit diagram we considered for our analysis is shown in Fig. 1. The operational principle of the circuit is discussed in [5], [6].

## II. Circuit Description

In the circuit, a hybrid bridge is used instead of a simple diode bridge. The hybrid bridge consists of two thyristors T1 and T2 and two diodes D1 and D2. $L$ is the inductance of superconducting coil. The inductance is varied from a lower value to a higher value to observe both load changing and fault situations. The positive half cycle of current flows through T1 and D1 and the negative half cycle through T2 and D2.

The advantage of using the hybrid bridge over the normal diode bridge is that it can also work as a fast solid state circuit breaker. In case of a high fault current, by removing the gate trigger pulses, the thyristors can shutdown the supply. "Load 1" and "Load 2" are connected in parallel. To observe the load changing effect, switch S2 is used to connect or disconnect the "Load 2." The solid state switch S1 is connected across the load terminal to make artificial fault.

## III. Waveform Analysis

Using EMTDC simulation tools we carried out the waveform analysis both in fault and load change conditions. We have considered a single phase 6.6 kV, 1 kA and 60 Hz system with 5 percent source impedance. The reactor's inductance value is assumed 1.0 pu. In Fig. 2, a sample of waveforms of voltage and current is obtained during load increasing time. In Fig. 3, the curves represents the voltage and current waveform of the same system during a fault time. In our analysis, after making

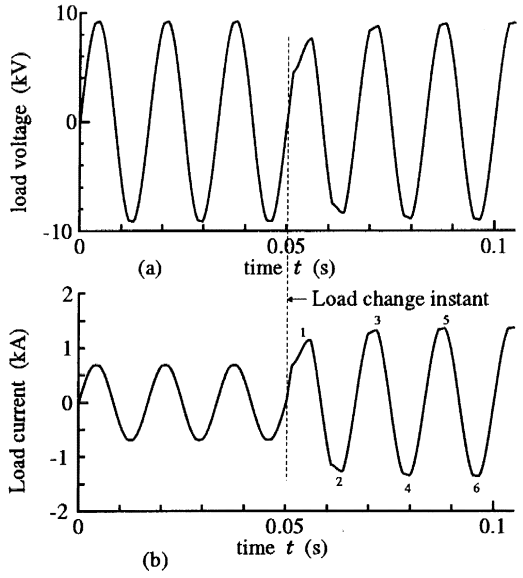


Fig. 2. Waveforms during load increasing time; Load is increased by 50 percent at 5.05 second instant. (a) Voltage. (b) Current waveform.

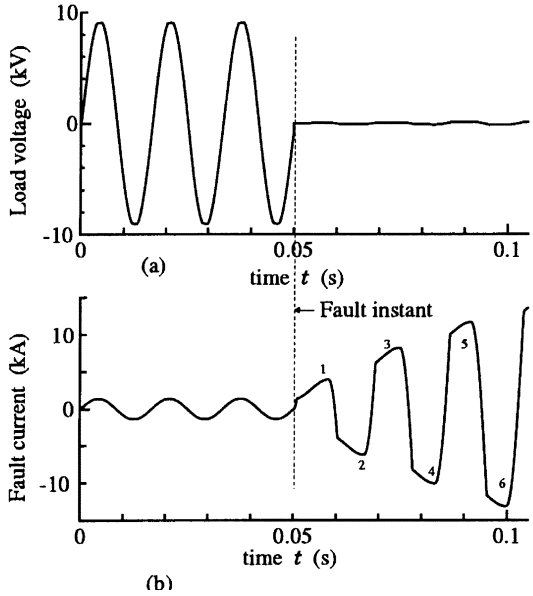


Fig. 3. Waveforms during fault time; Fault is made at 5.05 second instant. (a) Voltage. (b) Current waveform.

a load change or fault, we considered 6 consecutive peaks of the voltage or current waveforms. In Fig. 2 when the load is increased by 50 percent (in the diagram, a step change is made at 0.05 sec instant), the voltage dip appears in the voltage waveform. The voltage dip is higher in first peak (upper half cycle) than the 2nd peak (lower half cycle) and so on. In case of a fault shown in Fig. 3, the first peak (upper half cycle) of the fault current is smaller than the 2nd peak value (lower half cycle) and so on. We considered 6 such consecutive peak values for our analysis. By observing the numerical values at the EMTDC output channels, we obtained the peak value of each 6 half cycles. Both in the load change and fault time we adopted the same procedure to obtained the peak numerical values. We repeated the procedure at different inductance values.

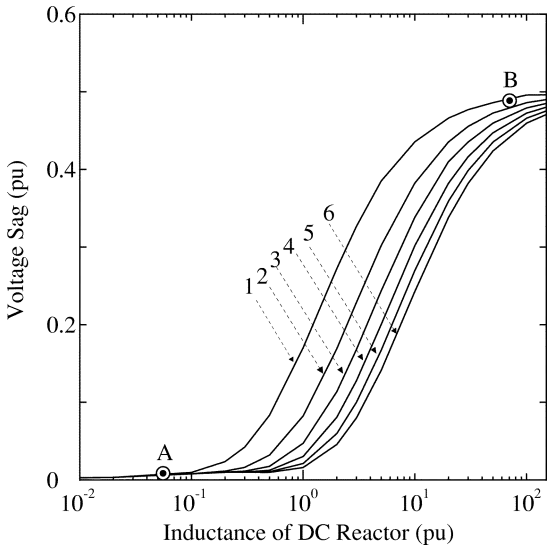


Fig. 4. Load increasing effect is shown in the figure. Higher value of inductance causes larger voltage sag. Traces marked 1 to 6 represents the individual effect of voltage sag of 6 consecutive half cycles after load is increased.

Because no DC bias is used in the rector coil, the voltage sag occurs on the voltage waveform at the load terminal when the load is increased. In Fig. 4 the graph shows the voltage dip during the load increasing time at different inductance values. In this case the load is changed up to 50 percent and the effect is observed on the 6 subsequent half cycles after the instant of the load change. To calculate the voltage sag we measured each peak value of the waveforms after the load is changed and divide its value by the peak value of normal waveform (before load is increased). The curves shows how the higher value of inductance effect on the output voltage. The trace marked 1 represents the voltage dip occurring in the first half cycle after the load change and trace 2 represents the same for 2nd half cycle and so on. The first half cycle suffers from highest voltage dip followed by the 2nd half cycle and so on. From the plot, in the case of the first half cycle, the voltage dip is approximately 15 percent at 1 pu inductance value when a step load is increased by 50 percent. So the plot gives us a real understanding to estimate the relationship between the voltage sag and inductance values. Points A and B represent the inductance values used in experiments [1], [2].

Fig. 5 represents the fault current to normal current ratio at different inductance values. In this case the fault is made at a zero crossing time of the current waveform. The ratio is obtained by dividing the peak fault value of each half cycle by the peak value of the normal current. As the fault current continues to increase, the ratio also increases for subsequent cycles after the fault is made. We measured up to 6 subsequent half cycles in order to calculate the fault current to normal current ratio. In the diagram the trace 1, trace 3 and trace 5 represent the ratio for the positive half cycles and trace 2, trace 4, and trace 6 represent for the negative half cycles. In trace 1 at lower inductance value, much higher ratio is observed. This is because, the DC shift occurs during the fault time. The diagram shows that the maximum DC shift of the first positive half cycle occurred at inductance value 0.01 pu. The trace 2 represents for the 1st neg-

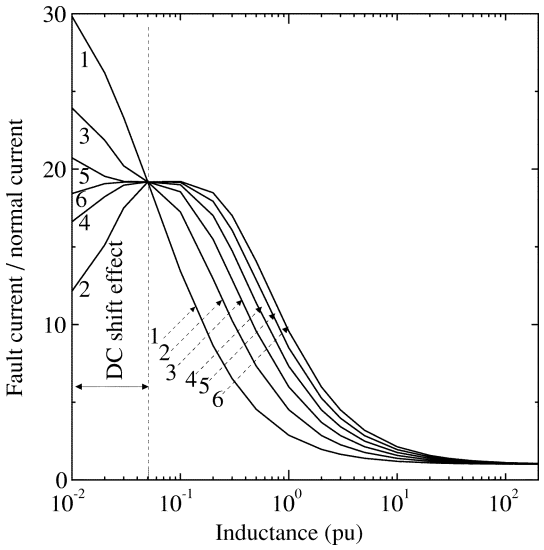


Fig. 5. Ratio of fault current to normal current is plotted at different inductance values. In this case fault is made at the zero crossing position of the current waveforms. DC shift effect appeared in 0.01 to 0.05 pu inductance range. DC shift is maximum in this situation.

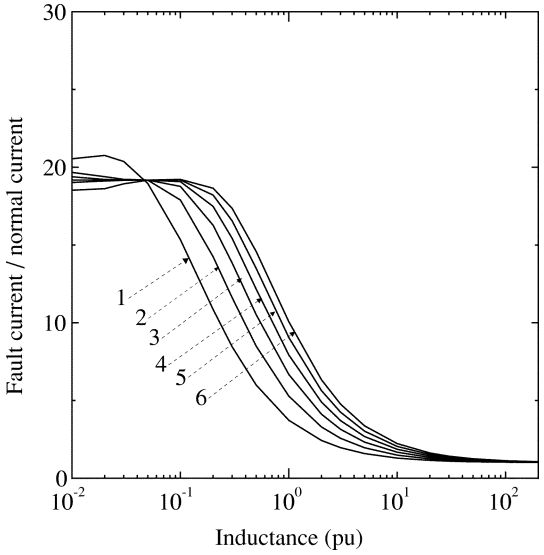


Fig. 6. Ratio of fault current to normal current is plotted at different inductance values. In this case fault is made at the peak value of the current waveforms. DC shift effect on the fault current is minimum in this situation.

ative half cycle of the 6 half cycles we considered. Due to the positive DC shift, the peak value of the negative half cycle is reduced with respect to the original time axis, therefore the fault to normal current ratio is reduced. This is true for all subsequent negative half cycles as are shown in trace 4 and trace 6 respectively. At an inductance value 0.05 pu, all the 6 half cycles show almost the same ratio which is a interesting part of this analysis. We took the data from 0.1 pu to 200 pu. As the inductance value increases as shown in the diagram, the ratio of fault current to normal current reduces. At very high inductance value the ratio becomes almost equal for all half cycles.

In Fig. 6 the graph represents the same as it is shown in Fig. 5, however in this case the fault is made at the peak of the current waveform. In such a case the DC shift is minimum. In the diagram it is shown that from 0.01 pu to 0.05 pu there is no significant difference of the fault to normal current ratio resulting from a DC shift. The other portion of the waveform i.e., from 0.05 pu to 200 pu of inductance is similar to those found in Fig. 5.

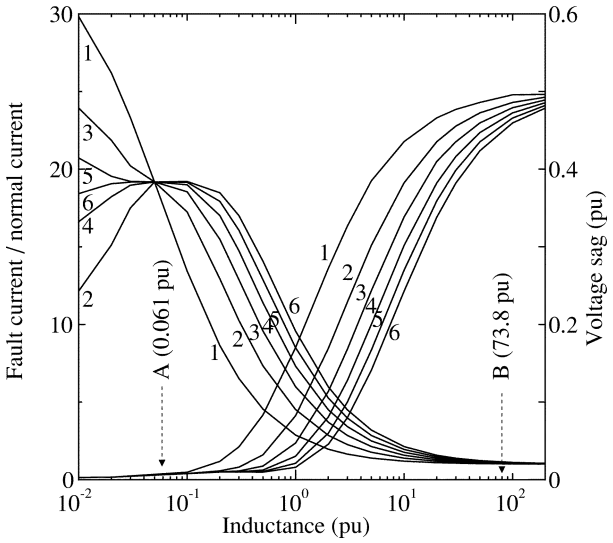


Fig. 7. Left side curves show the fault to normal current ratio and the right side curves show the voltage sag due to load increase. A suitable inductance value can be in the range of 0.7 to 1.2 pu where the maximum voltage sag is less than 20 percent and maximum fault to normal current is less than 10 times in the first half cycle.

Selecting a suitable inductance value for a bridge type SFCL is very important. The inductance value determines the fault to normal current ratio. Load increasing effects and DC shift is also dependent on inductance values. The diagrams obtained in Figs. 4 and 5 are compared on the same inductance axis in order to find out a suitable inductance value for the DC reactor of the current limiter. In the diagram shown in Fig. 7, the left side curves represent the fault to normal current ratio and right side curves represent voltage drop considering 50 percent load change in a 6.6 kV, 1 kA system. The left side curves tell us to select higher inductance value to avoid DC shift effect and higher fault to normal current ratio. On the other hand, the right side curves discouraging for higher inductance values because of the higher voltage drop at the load terminal. So we have to compromise between them. If we want a fault current less than 10 times the normal current in the first half cycle and maximum voltage sag is desired less than 20 percent, a suitable inductance value can be in the range of 0.7 pu to 1.2 pu. We projected practical inductance values (at A and B) on the simulation curves used in the experiments.

## IV. Experimental Results

We made experiments in lower rated voltage and current and observed the output results. The Table I below shows the specifications of the superconducting coil used in the experiment. We observed both the fault and load changing situations. A high value of inductance (73.82 pu) is used because it was readily available in our laboratory.

To make load changing test, the load is increased to double by switching the “Load 2” in Fig. 1. Fig. 8 shows the voltage and the current waveforms due to the load increase. Fig. 8(a) represents the voltage and Fig. 8(b) represents the load current

TABLE I
SPECIFICATION OF THE SUPERCONDUCTOR COIL

| Wire | NiTi/(Cu +CuNi) |
|---|---|
| Cu ratio | 1/3.3 |
| Coil hight | 219 mm |
| Inner diameter | $\phi$96 mm |
| Outer diameter | $\phi$168.5 mm |
| Rated Magnetic Field | 4.81 T |
| Stored Energy | 23.5 kJ |
| Inductance | 1.175 H |
| Maximum Voltage | 60 V |
| Maximum Current | 200 A |

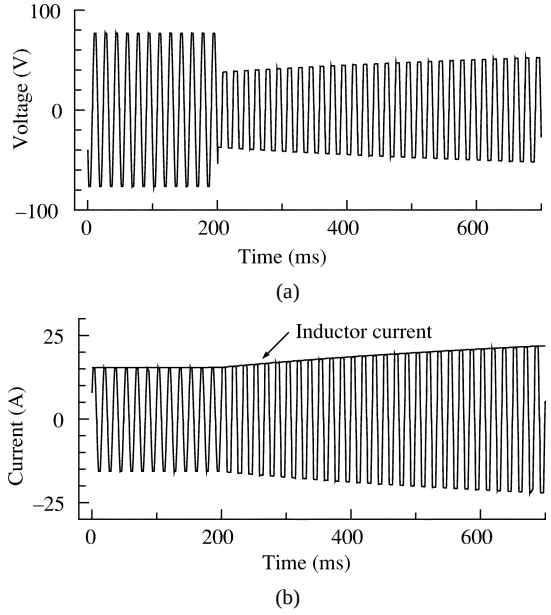


Fig. 8. Long term effect of load increasing. (a) Load voltage. (b) Load current and inductor current.

and the inductor current. The load voltage is suddenly reduced at the time of the load increase and it recovers exponentially. Load current and inductor current increase at the same rate which is clearly shown in Fig. 8(b).

To see the current limiting performance of the SFCL, an artificial fault is made by short-circuiting the load. This is made by turning on the solid state switch S1 of Fig. 1. Fig. 9 shows the output results when fault is made. The graph (a) represents the voltage waveform and graph (b) represents both the inductor current and fault current.

Solid-state switch S1 consists of thyristors connected in anti-parallel condition. When it is triggered to make a fault, the thyristors turn on, but turn off again at zero crossing point. It does not turn on until a threshold current is achieved. This is true even though the gate signal is continuously on. For this reason some voltage pulses appear near the zero crossing region at the time of the fault. In the test the fault duration time is selected at 20 cycles in order to see its long term effect. At this time the peak fault current reached only twice the normal peak current. This is because the higher value of inductance limits the fault current more effectively.

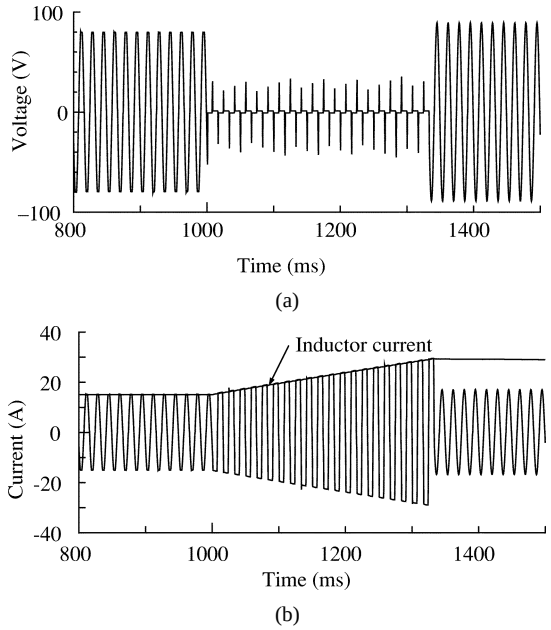


Fig. 9. Waveforms of long-period fault. Fault duration time is 20 cycles. (a) Voltage. (b) Fault current and inductor current.

## V. CONCLUSION

We have analyzed the voltage and current waveform of a bridge type SFCL in order to select a suitable inductance value for proper operation both in normal and current limiting mode. We have shown that at a very low inductance value a DC shift can have a big effect on the fault current and the maximum DC shift occurs when the fault is happens at the zero crossing of the current waveform. The fault to normal current ratio is much higher for a low inductance value. On the other hand, introducing higher inductance values reduce the fault current but cause voltage sags on the output voltage of the load terminal during load increasing period. Analyzing output waveforms obtained from simulation results, we explained a simple guideline how to select a suitable value for such a system. Some of our experimental results at very high inductance value are included to this paper as a reference.

## REFERENCES

[1] T. Yazawa *et al.*, "Design and test results of 6.6 kV high-Tc superconducting fault current limiter," *IEEE Trans. on Applied Superconductivity*, vol. 11, no. 1, pp. 2511–2514, March 2001.
[2] T. Hoshino K, M. Salim, M. Nishikawa, I. Muta, and T. Nakamura, "DC reactor effect on bridge type superconducting fault current limiter during load increasing," *IEEE Trans. on Applied Superconductivity*, vol. 11, no. 1, pp. 1944–1947, March 2001.
[3] ——, "Proposal of saturated DC reactor type Superconducting Fault Current Limiter (SFCL)," *Cryogenics*, vol. 41, pp. 469–474, 2001.
[4] K. M. Salim, T. Hoshino, M. Nishikawa, I. Muta, and T. Nakamura, "Preliminary experiments on saturated DC reactor type fault current limiter," *IEEE Transactions on Applied Superconductivity*, vol. 12, no. 1, pp. 872–875, March 2002.
[5] H. J. Boening and D. A. Paice, "Fault current limiter using superconducting coil," *IEEE Trans. on Magn.*, vol. MAG-19, no. 3, pp. 1051–1053, May 1983.
[6] T. Ishigohka *et al.*, "Fabrication and test of cryogenic fault current limiter combining semiconductors and DC reactor," *Proc. of IPEC-Tokyo 2000*, vol. 3, pp. 1525–1528, April 2000.